

DESCRIPTION

The 4406A is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance.

This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications

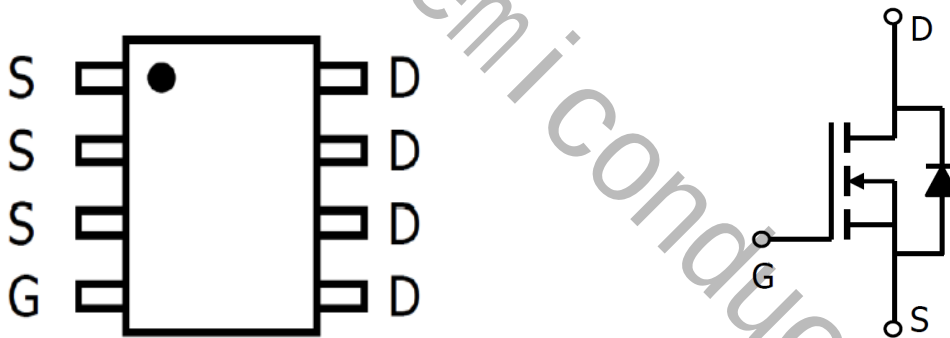
FEATURE

- ◆ 30V/15A, $R_{DS(ON)} = 8.5m\Omega$ (typ.)@ $V_{GS}=10V$
- ◆ 30V/11A, $R_{DS(ON)} = 14m\Omega$ (typ.)@ $V_{GS}=4.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOP8 package design

APPLICATIONS

- ◆ High Frequency Point-of-Load Synchronous
- ◆ Newworking DC-DC Power System
- ◆ Load Switch

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Continuous Drain Current (T _A =25℃)	V _{GS} =10V	15	A
	Continuous Drain Current (T _A =70℃)		12	a
I _{DM}	Pulsed Drain Current		40	A
I _S	Continuous Source Current (Diode Conduction)		2.0	A
P _D	Power Dissipation	T _A =25℃	3.0	W
		T _A =70℃	2.1	
T _J	Operation Junction Temperature		150	℃
T _{STG}	Storage Temperature Range		-55~+150	℃
R _{θJA}	Thermal Resistance Junction to Ambient		85	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

■ **ELECTRICAL CHARACTERISTICS**($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.0	1.9	3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0			1	uA
		V _{DS} =24V, V _{GS} =0 T _J =55°C			5	
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =15A		8.5	11	mΩ
		V _{GS} =4.5V, I _D =11A		14	18	
Source-Drain Diode						
V _{SD}	Diode Forward Voltage	I _S =1.0A, V _{GS} =0V		0.71	1.0	V
Dynamic Parameters						
Q _g	Total Gate Charge	V _{DS} =15V V _{GS} =4.5V I _D =14A		16	20.8	nC
Q _{gs}	Gate-Source Charge			5	6.5	
Q _{gd}	Gate-Drain Charge			3	3.9	
C _{iss}	Input Capacitance	V _{DS} =15V V _{GS} =0V f=1MHz		2470		pF
C _{oss}	Output Capacitance			325		
C _{rss}	Reverse Transfer Capacitance			185		
T _{d(on)}	Turn-On Time	V _{DS} =15V I _D =14A V _{GEN} =10V R _G =6Ω		17	34	nS
T _r				5	10	
T _{d(off)}	Turn-Off Time			50	100	
T _f				10	20	

Note: 1. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

2.Static parameters are based on package level with recommended wire bonding

■ TYPICAL CHARACTERISTICS (25 °C Unless Note)

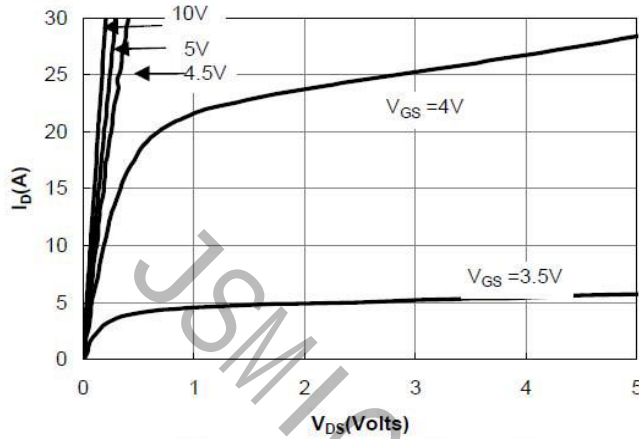


Figure 1: On-Regions Characteristics

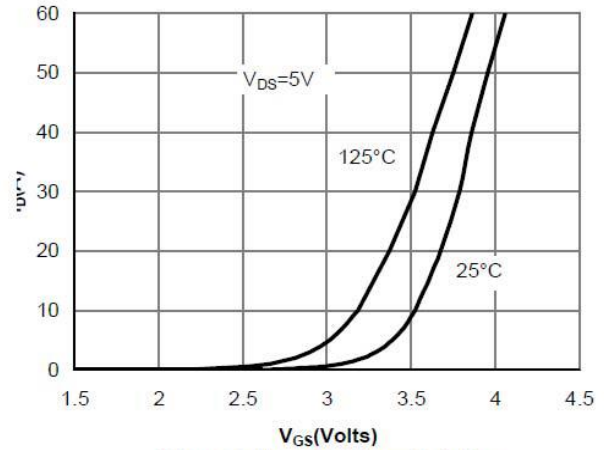


Figure 2: Transfer Characteristics

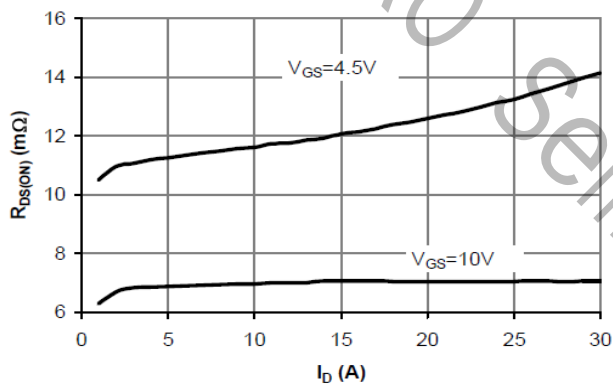


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

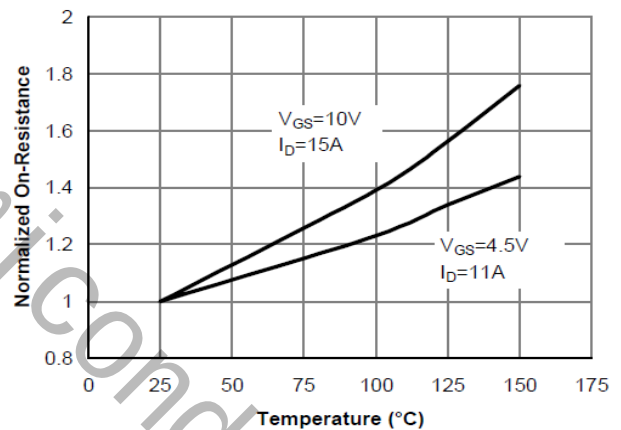


Figure 4: On-Resistance vs. Junction Temperature

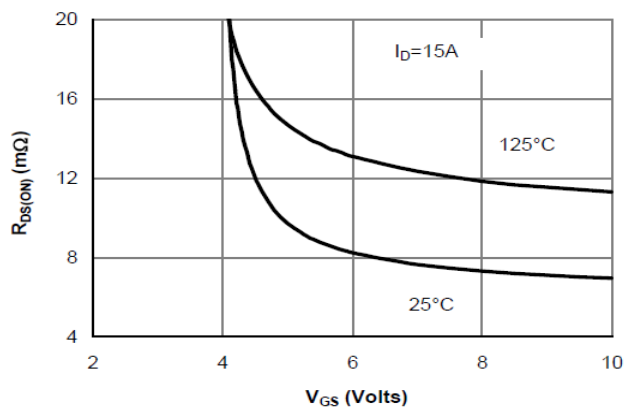


Figure 5: On-Resistance vs. Gate-Source Voltage

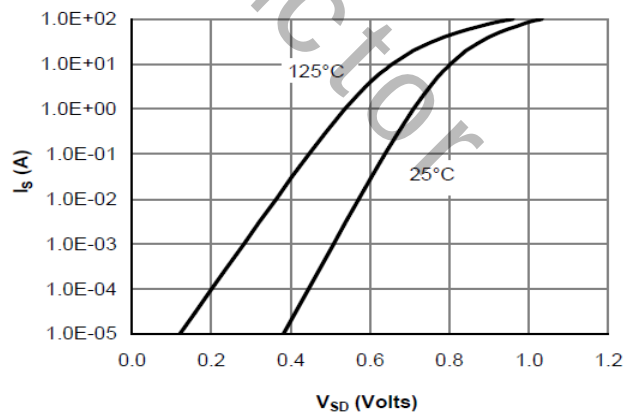


Figure 6: Body-Diode Characteristics

■ TYPICAL CHARACTERISTICS (continuous)

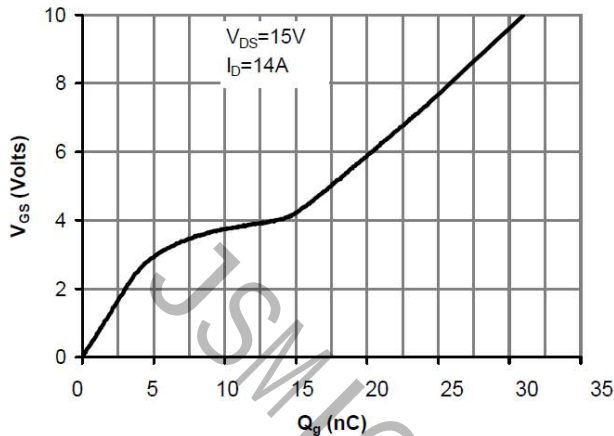


Figure 7: Gate-Charge Characteristics

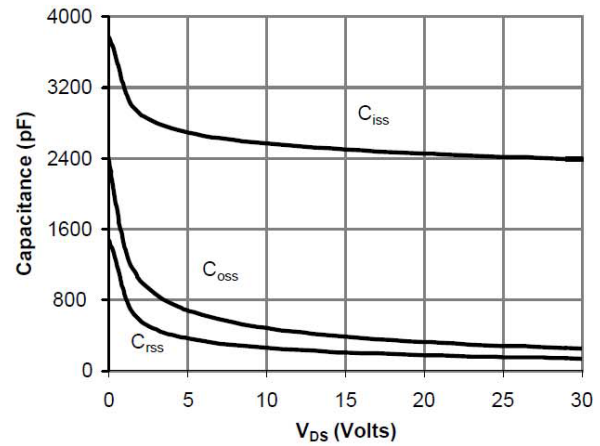


Figure 8: Capacitance Characteristics

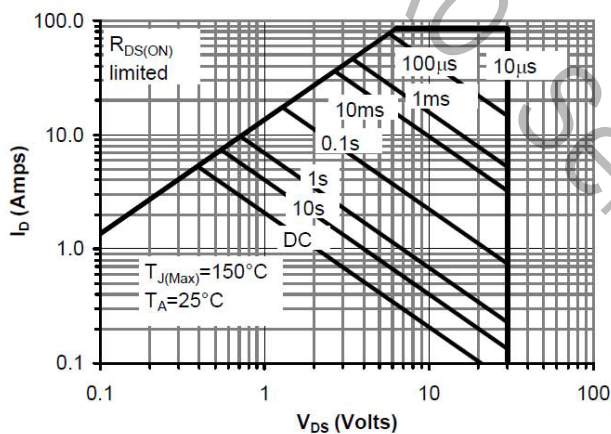


Figure 9: Maximum Forward Biased Safe Operating Area

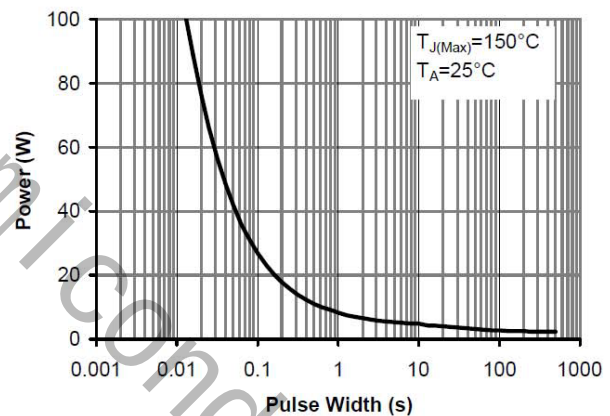


Figure 10: Single Pulse Power Rating Junction-to-Ambient

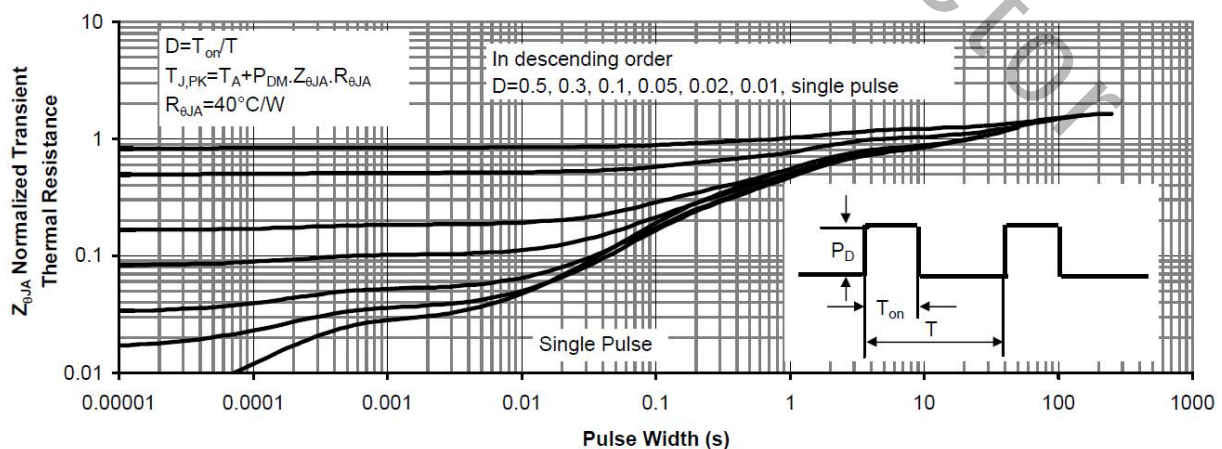
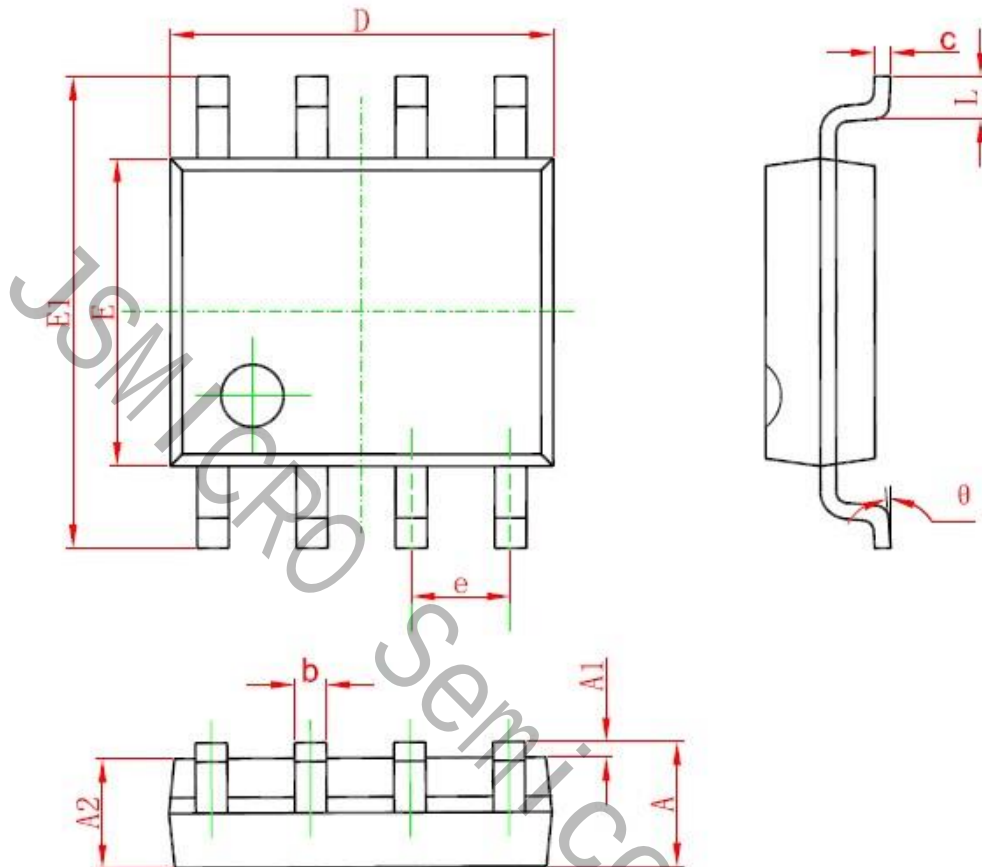


Figure 11: Normalized Maximum Transient Thermal Impedance

■ SOP8 PACKAGE OUTLINE DIMENSIONS

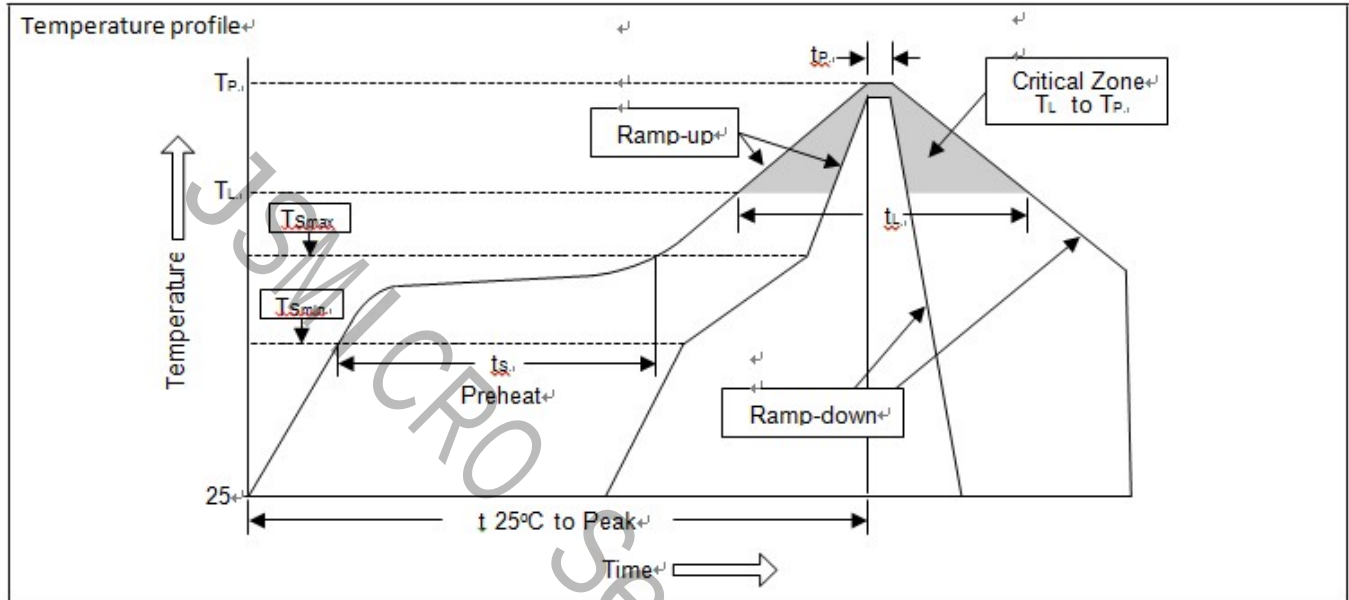


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

■ SOLDERING METHODS FOR UNIVERCHIP

Storage environment Temperature=10°C~35°C Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat		
-Temperature Min (T_{Smin})	100°C	150°C
-Temperature Max (T_{Smax})	150°C	200°C
-Time (min to max) (t_s)	60~120 sec	60~180 sec
T_{Smax} to T_L		
-Ramp-up Rate	<3°C/sec	<3°C/sec
Time maintained above		
-Temperature (T_L)	183°C	217°C
-Time (t_L)	60~150 sec	60~150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C±5°C	5sec±1sec
Pb-Free device	260°C +0/-5°C	5sec±1sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

JSMICRO Semiconductor